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PATENT
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Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of the claims in the application. All claims currently being amended are shown with deleted text struckthrough or double bracketed and new text underlined. Additionally, the status of each claim is indicated in parenthetical expression following the claim number.

Claims 1-20 remain.

Claims 8-15 are allowed.

Claims 7 and 18 – 20 stand objected-to.

Claims 1 – 6 and 16 – 17 stand rejected.

Claims 1, 2, and 16 are being amended

Claims 7 and 18 are being cancelled.

WHAT IS CLAIMED IS:

1. (Currently Amended) A debug subsystem for testing a system-on-a-chip including an embedded processor and memory comprising:

at least one sub-block operable to:

monitor a <u>data</u> bus between the processor and the memory to detect program selected triggering events, <u>the triggering events including predetermined data values appearing on the data bus</u>;

count the number of triggering events detected; and

when the number of triggering events reaches a program selected threshold, generating a debugging signal.

2. (Currently Amended) The debug subsystem of Claim 1 wherein the triggering events <u>further include</u> [[comprise]] memory accesses.

3. (Original) The debug subsystem of Claim 2 wherein the memory accesses are selected from the group including reads and writes.

4. (Original) The debug subsystem of Claim 2 wherein the triggering events comprise memory accesses within a selected address range.

5. (Original) The debug subsystem of Claim 1 wherein the debugging signal is operable to freeze a clock timing the operation of the processor.

6. (Original) The debug subsystem of Claim 1 wherein the debugging signal comprises an interrupt to the processor.

7. Cancelled

8. (Allowed) A system on a chip comprising:

at least one processor;

a plurality of memory spaces accessible by said processor via address and data buses; and

a debug block comprising a plurality of independently programmable debug sub-blocks each for monitoring accesses to a selected one of said memories and detecting triggering events, each sub-block comprising:

a first register for setting triggering event parameters;

a second register for setting a threshold number of triggering events;

a counter for maintaining a count of detected triggering events; and

circuitry for generating a control signal when the count reaches the threshold.

9. (Allowed) The system of Claim 8 wherein said triggering event parameters set in said first register select a selected one of the memories, select a memory access type and select an address range for detecting the access.

10. (Allowed) The system of Claim 8 wherein said triggering event parameters set in said first register select a value of data accessed from the selected one of the memories.

11. (Allowed) The system of Claim 9 wherein said control signal freezes a clock driving said processor.

12. (Allowed) The system of Claim 8 wherein said control signal comprises an interrupt to said processor.

13. (Allowed) The system of Claim 8 further comprising a second processor and said control signal comprises an interrupt to at least one of said processors.

14. (Allowed) The system of Claim 13 wherein said second processor can access said memories and generate trigger events.

15. (Allowed) The system of Claim 13 wherein said processor comprises a digital signal processor and said second processor comprises a microprocessor.

16. (Currently Amended) A method of debugging a single-chip system including an embedded processor and memory including a plurality of memory spaces, comprising the steps of:

selecting programmable triggering event parameters including selecting one of the memory spaces for monitoring;

monitoring transactions between the processor and the memory to detect triggering events corresponding to the selected triggering event parameters;

counting the number of triggering events detected; and

when the number of triggering events reaches a programmed predetermined threshold, generating a debugging signal.

17. (Currently Amended) The method of Claim 16 wherein said step of selecting triggering event parameters further comprises the substeps of:

selecting a triggering memory access type; and

selecting a triggering address range.

18. Cancelled

19. (Original) The method of Claim 16 wherein said step of monitoring comprises the step of monitoring an address bus to the memory for memory accesses meeting the triggering event parameters.

20. (Currently Amended) The method of Claim 16 wherein said step of selecting triggering event parameters further comprises the substep of selecting triggering events to step through code being run by the processor.